

## Notes on EE 2310 Test #2

### Conditions

1. As this is effectively a take-home test, it is considered fully open-book and open-notes. You may use notes taken in class, homeworks, lecture slides, etc.
2. No calculators will be needed (as usual).
3. ASCII codes will be provided if required in a problem.
4. When turning in the test, you must digitally sign (including UTD ID), verifying that you completed the test on your own, that is, without help from anyone else.

### Items Potentially Covered on the Test

1. Master-slave flip-flops (T, D, J-K).
2. Clocks and timing diagrams.
3. Synchronous (parallel) counters. Emphasis will be on counters!
4. Shift registers.
5. Diagnosing and describing the operation of a complex sequential circuit, which might be made up of both combinational and sequential circuits.
6. Combinational logic concepts (necessary with many sequential circuits).
7. Hexadecimal and binary arithmetic as needed to interpret assembly instructions.
8. All standard assembly instructions, including reg.-reg., shift and rotate, memory access (lw, sw, lb, sb), jump (j, jal, jr), branch (bne, bgtz, etc.). No “set” (such as slt) or shift.
9. Syscalls, directives, and use of labels.
10. Use of the stack.
11. More complex loop programs.
12. Basic computer architecture, concentrating mainly on the MIPS pipeline.
13. The concepts of hazards, forwarding, and stalls.
14. Showing how an instruction goes through the pipeline, including what control lines are active and register identifications that must accompany the partial calculations.
15. Branch decision-making and how the pipeline can be modified to eliminate much of the overhead of incorrect branch decisions.
16. Bonus questions as listed in the 35-question homework (most from Lectures 17-21). Five of these questions, exactly as shown in the 35-question list, will be on the test.

### Not on the Test:

Only those items specifically named above will be included in the test possibilities—and not all of them may be on the test.